Customer No. 22,852
Attorney Docket No. 04329.3105

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Tsutomu TEZUKA et al.	
Application No.: 10/628,513	Group Art Unit: 2812
Filed: July 29, 2003	Examiner: Not assigned
For: SEMICONDUCTOR DEVICE MANUFACTURING METHOD	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application .

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that the listed documents are material or constitute "prior art." If the Examiner applies the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

present to the office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: December 23, 2003

By: _____
Richard V. Burgujian
Reg. No. 31,744

Enclosures
RVB/FPD/dvg

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.3105	Application No.	
Applicant	Tsutomu TEZUKA et al.		
Filing Date	December 23, 2003	Group:	Not assigned

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	T. Tezuka et al., "Dislocation-free formation of relaxed SiGe-on-insulator layers", American Institute of Physics, (May 13, 2002)
	T. Tezuka et al., "Integrated Circuit Device", Application No.: 10/188,824, filed July 5, 2002.
	A. Nishida et al., "Elimination of misfit dislocations in $Si_{1-x}Ge_x$ /Si heterostructures by limited-area molecular-beam epitaxial growth", J. Appl. Phys. vol.71 (12), June 15, 1992.

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce